System and Method for Increasing the Speed of Serially Inputting Data into a JTAG-Compliant Device

ABSTRACT

A JTAG-compliant device is configured to receive data through the control (TMS) line in addition to being configured to receive data through the input (TDI) line. A burst-write instruction is made the active instruction, extending the capability of the test access protocol (TAP) controller such that the TAP controller can receive data into a data register while the TAP controller is in certain states. In some states, the TAP controller receives and stores a bit only from the input line. In other states, the TAP controller receives and stores a bit from the input line, and in addition, the TAP controller receives and stores a bit from the control line. The TAP controller may store the received bits by shifting the received bits into the least significant bit of a data register.